AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace the paragraph beginning on page 15, line 10 with the following rewritten paragraph:

- - Referring now to the figures of the drawings in detail and first, particularly to Fig, 6 thereof, there is shown a customary layout of a planar light circuit 5 (PLC) for the purposes of better understanding of the invention. To manufacture the PLC, a plurality of SiO_3 layers having various refractive indices are deposited on a silicon wafer 51. These layers are a buffer layer 52, a core layer (not shown), and a top layer 53. The core layer, situated between the buffer layer and the top layer, has the largest refractive index in this case. Before the core layer is covered with the top layer 53, a photolithographically produced mask (e.g.. AZ resist) and an etching method (e.g. RIE - Reactive Ion Etching) are used to structure the core layer such that only individual ribs 54 of this layer remain. These ribs 54 are then covered with the top layer 53 and form the light-carrying waveguide core. This core is disposed at a depth of approximately 20 jam in the SiO_2 layer system, which is approximately 4 0 um thick, and typically has a cross section of approximately 6 x 6 μm - -

Please replace the paragraph beginning on page 16, line 10 with the following rewritten paragraph:

- - An inventive detection unit [[1]] is shown in Fig, 1. A cutout or a trench 6, which interrupts the waveguide 54, is formed in the SiO_2 layer (corresponding to the top layer 53 and the buffer layer 52 in Fig. 6) and up to the silicon wafer for the purpose of detecting an optical signal running in a waveguide or waveguide core 54. The trench 6 is preferably produced using an etching method. For trench etching, it is an obvious measure to etch the trenches at a depth of

approximately 100 um, since this deep etching step is also performed for other function structures, for example in attenuator apparatuses - -

Please replace the paragraph beginning on page 18, line 23 with the following rewritten paragraph:

- - The manufacture and exact construction of the units of the detection configuration [[1]] are explained below with reference to Figs. 3a-3h. In this context, Figs. 3a to 3d are first used to describe the manufacture of the submount 7. First, a gold metalization is put onto the submount and a photolithographically produced mask (e.g. AZ resist) and an etching method [[are]] is used to structure said gold metalization, so that solder pads and conductor tracks are provided for the photodiodes and solder bumps (Figs. 3a and 3b). Next a passivation and soldering stop layer, e.g. Cyclotene, is spun on, structured and fixed. A template is then used in a screen printing method to spray on lead/tin spherical indentations (Fig. 3c). These are briefly heated so that they become round. Alternatively, "stud bumps" made of gold or gold/tin are put on as solder bumps.- -